IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1-3 and 8-10 as follows:

1. (Currently Amended) A memory device for driving a display panel comprising:

arrays of memory cells storing binary information;

pairs of bit line-bit bar line connected to the memory cells;

first transfer gates connected to one end of the bit line-bit bar line pairs and switched by a column address to access the memory cells;

second transfer gates connected to the other end of bit line-bit bar line pairs and switched to read out the binary information stored in the memory cells; and

data buffers to receive the read-out binary information of the memory cells from the second transfer gates, by the switching operation of the second transfer gates and to store the read-out binary information,

wherein signals switching the second transfer gates are derived from a single enable signal and divided into several groups, and the signal for each group has a different time delay.

2. (Currently Amended) A memory device for driving a display panel comprising:

a memory cell array storing binary information;

pairs of bit line-bit bar line connected to the memory cells;

first transfer gates connected to one end of the bit line-bit bar line pairs and

switched by a column address to access the memory cells;

second transfer gates connected to the other end of bit line-bit bar line pairs and switched to read out the binary information stored in the memory cells; and

data buffers to receive the read-out binary information of the memory cells from the second transfer gates, by the switching operation of the second transfer gates and to store the read-out binary information,

wherein signals enabling the data buffers are derived from a single enable signal and divided into several groups, and the signal for each group has a different time delay.

3. (Currently Amended) A memory device for driving a display panel comprising:

a memory cell array storing binary information;

pairs of bit line-bit bar line connected to the memory cells;

first transfer gates connected to one end of the bit line-bit bar line pairs and switched by a column address to access the memory cells;

second transfer gates connected to the other end of bit line-bit bar line pairs and switched to read out the binary information stored in the memory cells; and

data buffers to receive the read-out binary information of the memory cells from the second transfer gates, by the switching operation of the second transfer gates and to store the read-out binary information,

wherein signals enabling the data buffers and signals switching the second transfer gates are derived from a single enable signal and divided into several groups, and the signal for each group has a different time delay.

4. (Previously Presented) The memory device of claim 1, wherein the different time delay is performed by a circuit including a logic circuit having an inversing function.

5. (Previously Presented) The memory device of claim 1, wherein the different time delay is performed by a capacitor, a resistor, or a combination of the capacitor

and the resistor.

6. (Previously Presented) The memory device of claim 1, wherein the first transfer gates are switched by the column address as being grouped by unit of 2^n, wherein n is a positive integer including 0.

7. (Previously Presented) The memory device of claim 1, wherein the time delay is a signal generated by a plurality of delay portions which are connected in series.

8. (Currently Amended) A method of driving a memory device for driving a display panel, wherein data is written on a memory cell array through first transfer gates which are connected to one end of bit lines and partially selected and switched by a column address, the method comprising:

performing a switching operation of second transfer gates connected to the other end of the bit lines to read the written data on the memory cell array; and

transferring the written data ~~is transferred~~ from the second transfer gates to data buffers by a the switching operation of the second transfer gates connected to the other end of the bit lines, and

wherein the switching operation of the second transfer gates are performed by a signal divided into groups and having a different time delay.

9. (Currently Amended) A method of driving a memory device for driving a display panel, wherein data is written on a memory cell array through first transfer gates which are connected to one end of bit lines and partially selected and switched by a column address, the method comprising:

performing a switching operation of second transfer gates connected to the other end of the bit lines to read the written data on the memory cell array; and

transferring the written data ~~is transferred~~ to data buffers from the second transfer gates, by performing ~~a~~ the switching operation of the second transfer gates connected to the other end of the bit lines, and

wherein signals instructing to store the transferred data in the data buffers are divided into groups and have different time delays.

10. (Currently Amended) A method of driving a memory device for driving a display panel, wherein data is written on a memory cell array through first transfer gates which are connected to one end of bit lines and partially selected and switched by a column address, the method comprising:

performing a switching operation of second transfer gates connected to the other end of the bit lines to read the written data on the memory cell array; and

transferring the written data ~~is transferred~~ to data buffers by performing a~~the~~ switching operation of the second transfer gates connected to the other end of the bit lines, and

wherein the second transfer gates and the data buffers corresponding to the second transfer gates are simultaneously operated by signals divided into groups and having different time delays.

11. (Previously Presented) The method of claim 8, wherein the different time delay is performed by a circuit including a logic circuit having an inversing function.

12. (Previously Presented) The method of claim 8, wherein the different time delay is performed by a capacitor, a resistor, or a combination of the capacitor and the resistor.

13. (Previously Presented) The method of claim 8, wherein the first transfer gates are switched by the column address as being grouped by unit of 2^n, wherein n is a positive integer including 0.

14. (Previously Presented) The method of claim 8, wherein the time delay is a signal generated by a plurality of delay portions which are connected in series.

15. (Previously Presented) The memory device of claim 2, wherein the

different time delay is performed by a circuit including a logic circuit having an inversing function.

16. (Previously Presented) The memory device of claim 3, wherein the different time delay is performed by a circuit including a logic circuit having an inversing function.

17. (Previously Presented) The memory device of claim 2, wherein the different time delay is performed by a capacitor, a resistor, or a combination of the capacitor and the resistor.

18. (Previously Presented) The memory device of claim 3, wherein the different time delay is performed by a capacitor, a resistor, or a combination of the capacitor and the resistor.

19. (Previously Presented) The memory device of claim 2, wherein the first transfer gates are switched by the column address as being grouped by unit of 2^n, wherein n is a positive integer including 0.

20. (Previously Presented) The memory device of claim 3, wherein the first transfer gates are switched by the column address as being grouped by unit of 2^n, wherein n is a positive integer including 0.

21. (Previously Presented) The memory device of claim 2, wherein the time delay is a signal generated by a plurality of delay portions which are connected in series.

22. (Previously Presented) The memory device of claim 3, wherein the time delay is a signal generated by a plurality of delay portions which are connected in series.

23. (Previously Presented) The method of claim 9, wherein the different time delay is performed by a circuit including a logic circuit having an inversing function.

24. (Previously Presented) The method of claim 10, wherein the different time delay is performed by a circuit including a logic circuit having an inversing function.

25. (Previously Presented) The method of claim 9, wherein the different time delay is performed by a capacitor, a resistor, or a combination of the capacitor and the resistor.

26. (Previously Presented) The method of claim 10, wherein the different time delay is performed by a capacitor, a resistor, or a combination of the capacitor and the resistor.

27. (Previously Presented) The method of claim 9, wherein the first transfer gates are switched by the column address as being grouped by unit of 2^n, wherein n is a positive integer including 0.

28. (Previously Presented) The method of claim 10, wherein the first transfer gates are switched by the column address as being grouped by unit of 2^n, wherein n is a positive integer including 0.

29. (Previously Presented) The method of claim 9, wherein the time delay is a signal generated by a plurality of delay portions which are connected in series.

30. (Previously Presented) The method of claim 10, wherein the time delay is a signal generated by a plurality of delay portions which are connected in series.